

ABSTRACT OF THE DISCLOSURE

An interleaving method and apparatus provides parallel access in a linear and interleaved order to a predetermined number of stored data samples. A memory array with a plurality of memory devices is addressed by applying a first portion of an address to memory devices and by using a second portion of the address to select at least one memory device to be accessed, wherein the position of the first and second portions within the address is changed in response to a change between the linear order and the interleaved order. Due to the fact that the memory array is split into several individually addressable memory devices, each of these memory devices can be accessed in a linear and interleaved order by changing an allocation of a chip selection portion and a chip addressing portion of the address.